WHAT IS CLAIMED IS:

1. An electronic device, comprising:

a first conductive channel;

a second conductive channel; and

an isolation layer formed from and over said first conductive channel, interposing said first conductive channel and said second conductive channel and configured both to isolate said second conductive channel electrically from said first conductive channel and transfer momentum between charge carriers in said first conductive channel and charge carriers in said second conductive channel.

2. The electronic device as recited in Claim 1 wherein said first conductive channel interposes a first source and a first drain and a first gate is associated with said first conductive channel.

3. The electronic device as recited in Claim 1 wherein said second conductive channel interposes a first source and a second drain and a second gate is associated with said second conductive channel.

4. The electronic device as recited in Claim 1 wherein said

electronic device is a CMOS device, said isolation layer comprises silicon dioxide and said second conductive channel comprises a polysilicon MOS gate material.

5. The electronic device as recited in Claim 1 wherein said first conductive channel is over said second conductive channel.

6. The electronic device as recited in Claim 1 wherein said first conductive channel is coupled to a first circuit, said second conductive channel is coupled to a second circuit and said transfer of said momentum causes a current to flow in said second circuit as a function of a current flow in said first conductive channel.

7. The electronic device as recited in Claim 1 wherein said first conductive channel is coupled to a first circuit and said transfer of said momentum causes a voltage to exist across said second conductive channel as a function of a current flow in said first conductive channel.

8. A method of manufacturing an electronic device, comprising:

forming a first conductive channel;

forming an isolation layer from and over said first conductive channel; and

forming a second conductive channel proximate said isolation layer, said isolation layer configured both to isolate said second conductive channel electrically from said first conductive channel and transfer momentum between charge carriers in said first conductive channel and charge carriers in said second conductive channel.

9. The method as recited in Claim 8 wherein said electronic device is a CMOS device and said forming said first conductive channel is carried out using a CMOS tub diffusion process.

10. The method as recited in Claim 8 wherein said first conductive channel interposes a first source and a first drain and a first gate is associated with said first conductive channel.

11. The method as recited in Claim 8 wherein said second conductive channel interposes a first source and a second drain and a second gate is associated with said second conductive channel.

12. The method as recited in Claim 8 wherein said isolation layer is about 17 angstroms thick.

13. The method as recited in Claim 8 wherein said forming said second conductive channel comprises forming said second conductive channel over said first conductive channel.

14. The method as recited in Claim 8 wherein said first conductive channel is coupled to a first circuit, said second conductive channel is coupled to a second circuit and said transfer of said momentum causes a current to flow in said second circuit as a function of a current flow in said first conductive channel.

15. The method as recited in Claim 8 wherein said first conductive channel is coupled to a first circuit and said transfer of said momentum causes a voltage to exist across said second conductive channel as a function of a current flow in said first conductive channel.

16. An integrated circuit, comprising:

a substrate;

a first circuit supported by said substrate and configured to carry a current;

a second circuit; and

an electronic device, including:

a first conductive channel supported by said substrate and coupled to said first circuit,

a second conductive channel supported by said substrate and coupled to said second circuit, and

an isolation layer formed from and over said first conductive channel, interposing said first conductive channel and said second conductive channel and configured both to isolate said second conductive channel electrically from said first conductive channel and transfer momentum between charge carriers in said first conductive channel and charge carriers in said second conductive channel.

17. The integrated circuit as recited in Claim 16 wherein said first conductive channel interposes a first source and a first drain and a first gate is associated with said first conductive channel.

18. The integrated circuit as recited in Claim 16 wherein

said second conductive channel interposes a first source and a second drain and a second gate is associated with said second conductive channel.

19. The integrated circuit as recited in Claim 16 wherein said second circuit is supported by said substrate.

20. The integrated circuit as recited in Claim 16 wherein said transfer of said momentum causes a current to flow in said second circuit as a function of a current flow in said first conductive channel.

21. The integrated circuit as recited in Claim 16 wherein said transfer of said momentum causes a voltage to exist across said second conductive channel as a function of a current flow in said first conductive channel.

22. The integrated circuit as recited in Claim 16 further comprising further electronic devices supported by said substrate, each including one of said first conductive channel, one of said second conductive channel and one of said interposed isolation layer, said electronic device and said further electronic devices coupled in parallel to said first circuit and coupled in series to said second circuit.